

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

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- 1 1. (Currently Amended) A method comprising:
2 receiving real-time analog data at a personal computer implementing a general
3 purpose operating system;
4 generating a real-time ~~event~~ interrupt ~~at the personal computer~~ indicating a
5 request to process the real time data at a central processing unit (CPU);
6 determining whether the real-time ~~event~~ interrupt has a higher priority than a ~~first~~
7 non-real time ~~event~~ operation being processed at the ~~personal computer~~ CPU; and
8 processing the real-time data if the real-time ~~event~~ interrupt has a higher priority
9 than the ~~first~~ non-real time ~~event~~ operation.
 - 1 2. (Currently Amended) The method of claim 1 further comprising continuing to
2 process the ~~first~~ non-real time ~~event~~ operation if the real-time ~~event~~ interrupt does not
3 have a higher priority than the non- real time first event operation.
 - 1 3. (Currently Amended) The method of claim 1 further comprising:
2 saving the state of the ~~first~~ non-real time ~~event~~ operation at the personal computer
3 prior to processing the data associated with the real-time ~~event~~ interrupt; and
4 processing the ~~first~~ non-real time ~~event~~ operation after processing of the data
5 associated with the real-time ~~event~~ interrupt has been completed.
 - 1 4. (Currently Amended) The method of claim 1 further comprising:

2 receiving a ~~second~~ non-real time event interrupt while processing the real-time
3 event interrupt; and

4 determining whether the ~~second~~ non-real time event interrupt has a higher priority
5 than the real-time event interrupt.

1 5. (Currently Amended) The method of claim 4 further comprising:

2 continuing the processing of the real-time event interrupt if the ~~second~~ non-real
3 time event interrupt does not have a higher priority than the real time event interrupt.

1 6. (Currently Amended) The method of claim 4 further comprising:

2 terminating the processing of the real-time event interrupt if the ~~second~~ non-real
3 time event interrupt has a higher priority; and
4 processing the ~~second~~ non-real time event interrupt.

1 7. (Currently Amended) A computer system comprising:

2 a chipset;
3 a bus coupled to the chipset; and
4 a central processing unit (CPU), coupled to the bus, to generate a real-time event
5 interrupt upon receiving real-time analog data at the computer system and to process data
6 associated with the real-time event interrupt if the real-time event interrupt has a higher
7 priority than a non-real-time event operation currently being processed.

1 8. (Currently Amended) The computer system of claim 7 wherein the CPU
2 comprises:
3 a timer to generate timing signals at predetermined time intervals; and
4 an event mechanism coupled to the timer to generate the real time ~~events~~
5 interrupts.

9/ 1 9. (Currently Amended) The computer system of claim 8 wherein the CPU further
2 comprises an event handler coupled to the event mechanism to process the real-time
3 ~~events~~ interrupts.

1 10. (Original) The computer system of claim 9 wherein the CPU further
2 comprises a register coupled to the event mechanism to store real-time data.

1 11. (Currently Amended) The computer system of claim 9 wherein the event
2 mechanism determines the relative priority between the real-time ~~events~~ interrupts and
3 the non-real-time ~~events~~ operations.

1 12. (Original) The computer system of claim 11 wherein the CPU further
2 comprises an analog to digital converter coupled to the register.

1 13. (Currently Amended) A central processing unit (CPU) comprising:
2 a timer to generate timing signals at predetermined time intervals;
3 a register ~~coupled to the event mechanism~~ to store real-time data received at the
4 CPU as analog data;
5 an event mechanism coupled to the timer and the register to generate real time
6 ~~events~~ interrupts in response to receiving the timing signals and determining that real-
7 time data is stored within the register; and
8 an event handler coupled to the event mechanism to process data associated with
9 the real-time ~~events~~ interrupts received from the event mechanism upon determining the
10 relative priority between the real-time ~~events~~ interrupts and non-real-time ~~events~~
11 operations being processed.

1 14. (Previously Presented) The CPU of claim 13 wherein the real-time analog
2 data is data received from an analog radio coupled to the CPU.

1 15. (Currently Amended) The CPU of claim 13 wherein the event handler verifies
2 whether there is data stored in register upon detecting a real-time ~~event~~ interrupt and
3 determines the priority of the real-time ~~event~~ interrupt relative to other interrupts
4 received.

1 16. (Previously Presented) The CPU of claim 13 wherein the CPU further
2 comprises an analog to digital converter coupled to the register to convert the real-time
3 analog data to digital data.

1 17. (Previously Presented) The method of claim 1 wherein receiving the real-
2 time analog data comprises:
3 converting the real-time analog data to digital data; and
4 storing the digital data at a register.

91 1 18. (Currently Amended) The method of claim 17 wherein generating the real-time
2 ~~event~~ interrupt comprises:
3 receiving a timing signal at an event mechanism at a predetermined interval;
4 the event mechanism determining whether data is stored within the register; and
5 generating the real-time ~~event~~ interrupt if data is stored within the register

1 19. (Currently Amended) The computer system of claim 10 wherein the event
2 mechanism generates the real time ~~events~~ interrupts in response to receiving the timing
3 signals from the timer and determining that real-time data is stored within the register.

20. (Previously Presented) The computer system of claim 7 wherein the real-
time analog data is data received from an analog radio.
